CLAIMS AS ALLOWED

1. A method of modeling a digital processor comprising the steps of:

in a high level programming language, defining operations and data representations of a target processor, the operations and data representations being used in commands for execution by the target processor; and

in a computer system, using the defined operations and data representations, simulating the target processor executing certain commands to provide a model of the target processor data representations and operations, said simulating including generating model data indicative of results of the target processor having executed the certain commands, said generated model data providing a bit level representation of the target processor results.

2. A method as claimed in Claim 1 wherein the step of simulating includes providing the model generated data in human readable terms instead of machine code.

3. A method as claimed in Claim 1 further comprising the step of executing working code on the target processor, such that said target processor generates working data, and

wherein the step of simulating includes generating model data corresponding to the working data generated by the target processor in a manner such that the model data is (i) bit-wise matchable to the target processor generated working data, and (ii) in human readable terms.

4. A method as claimed in Claim 1 wherein the step of simulating further includes using the high level programming language, defining data types for the data representations of the target processor.

5. A method as claimed in Claim 4 wherein the step of simulating further comprises the steps of:

for a given source processor, (a) determining each distinct fixed bit length data representation, and (b) grouping the determined distinct data representation to form a set;

for each target processor, repeating steps (a) and (b) such that respective sets are formed; and

forming a hierarchy of the formed sets by correlating one set to another such that a base class with depending subclasses are generated and form the hierarchy, each set being defined by one of the base class and a subclass.

6. A method as claimed in Claim 4 wherein the step of defining operations is incremental such that one target processor operation at a time is defined and modeled using the high level programming language.

7. A method as claimed in Claim 1 further comprising the step of generating diagnostic data corresponding to said simulating.

8. A method as claimed in Claim 7 wherein said step of generating diagnostic data includes indicating number of times different operations of the target processor are encountered during said simulating.

9. A method as claimed in Claim 1 wherein the step of simulating is incremental, such that a first set of certain data representations and operations of the target processor is simulated using the high level programming language to form an intermediate model of the target processor, and subsequent to the formation of the intermediate model, at least a second set of data representations and operations of the target processor is simulated using the high level programming language to increment the intermediate model toward a final desired model of the target processor.

10. Computer apparatus for modeling a digital processor, comprising

a set of high level programming language definitions of data representations and operations of a target processor, the operations and data representations being used in commands for execution by the target processor; and

a modeling routine coupled to the set, the modeling routine using a high level programming language and simulating the target processor executing certain commands to provide a model of the data representations and operations of the target processor, the modeling routine generating model data indicative of results of the target processor having executed the certain commands, said generated model data providing a bit level representation of the target processor results.

11. Apparatus as claimed in Claim 10 wherein the modeling routine generates model data which is in human readable terms instead of machine code.

12. Apparatus as claimed in Claim 10 further comprising a set of data types defined for the data representations of the target processor using the high level programming language.

13. Apparatus as claimed in Claim 12 wherein the set is formed by the steps of:

for a given source processor, (a) determining each distinct fixed bit length data representation, and (b) grouping the determined distinct data representation to form a working set;

for each target processor, repeating steps (a) and (b) such that respective working sets are formed; and

forming a hierarchy of the working sets by correlating one set to another, such that a base class with depending subclasses are generated and form the hierarchy, each working set being defined by one of the base class and a subclass.

14. Apparatus as claimed in Claim 12 wherein the modeling routine enables target processor operations to be defined incrementally, such that one target processor operation at a time is defined and modeled using the high level programming language.

15. Apparatus as claimed in Claim 10 wherein the set further includes definitions of diagnostic operations; and

further comprising a diagnostic subroutine coupled between the source and the modeling routine, the diagnostic subroutine generating diagnostic data corresponding to said simulating by the modeling routine.

16. Apparatus as claimed in Claim 15 wherein the diagnostic data includes number of times different operations of the target processor are encountered during said simulating by the modeling routine.

17. Apparatus as claimed in Claim 10 wherein the modeling routing models the target processor incrementally, such that the modeling routine simulates a first set of certain data representations and operations of the target processor using the high level programming language, to form an intermediate model of the target processor, and subsequent to the formation of the intermediate model, the modeling routing simulates at least a second set of data representations and operations of the target processor using the high level programming language, to increment the intermediate model toward a final desired model of the target processor.